

FIG. 1

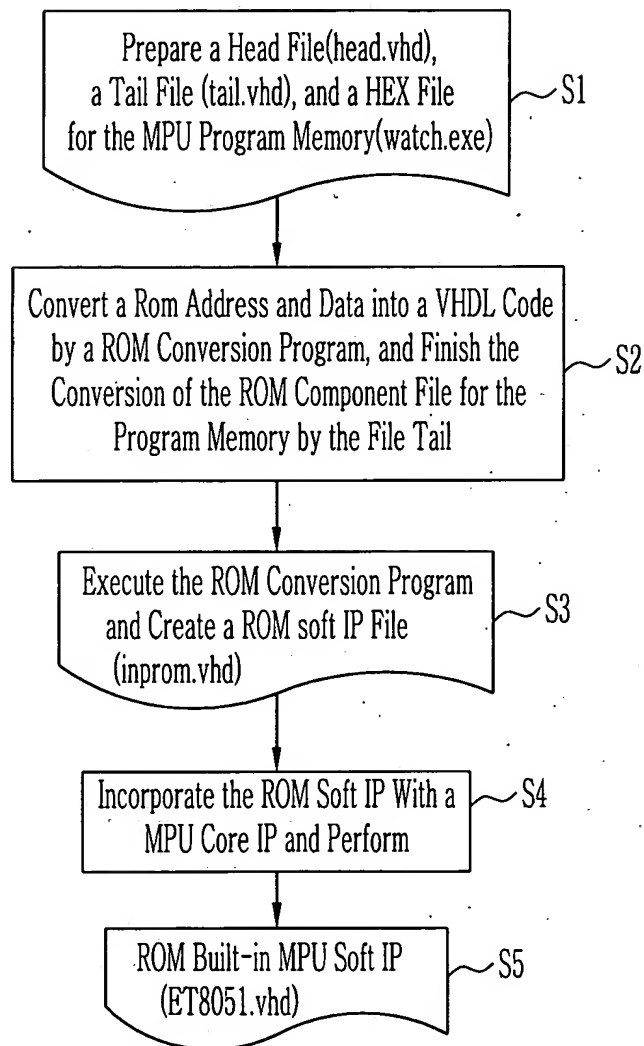


FIG. 2

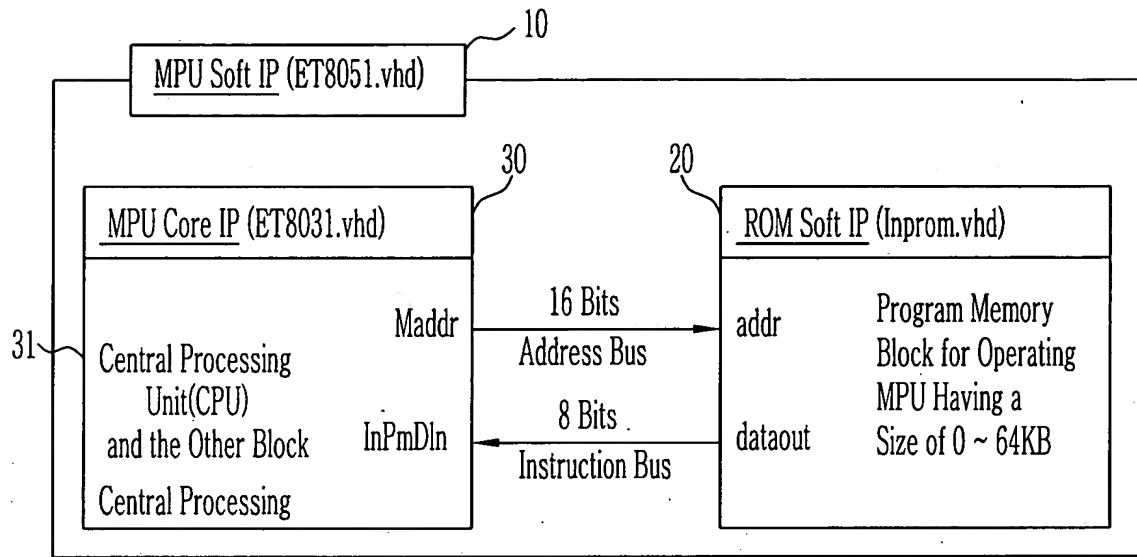


FIG. 3

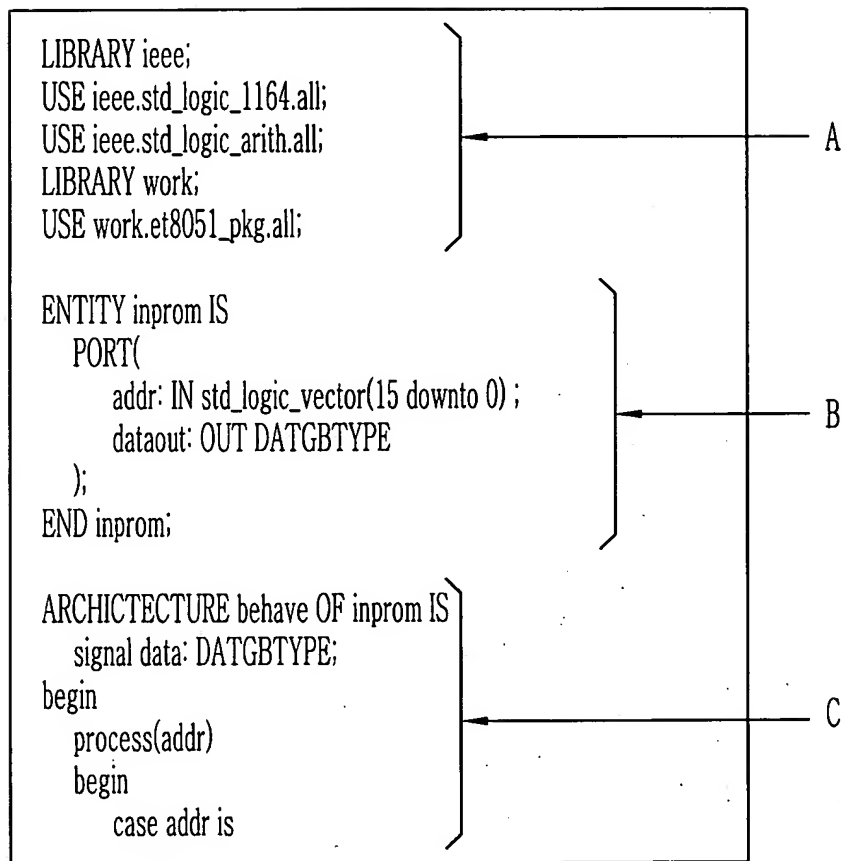


FIG. 4

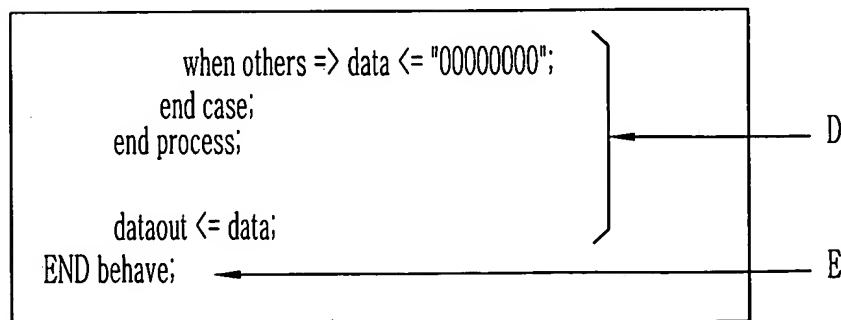


FIG. 5

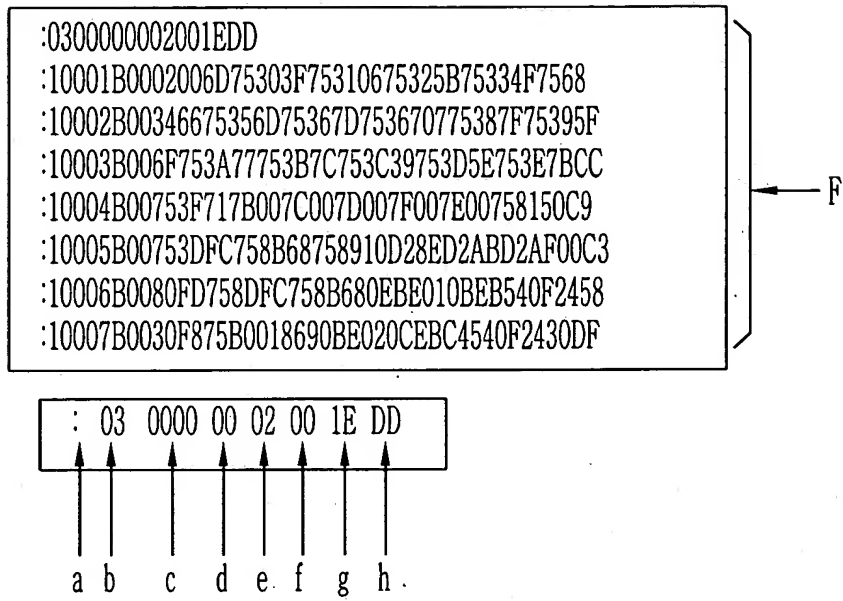


FIG. 6A

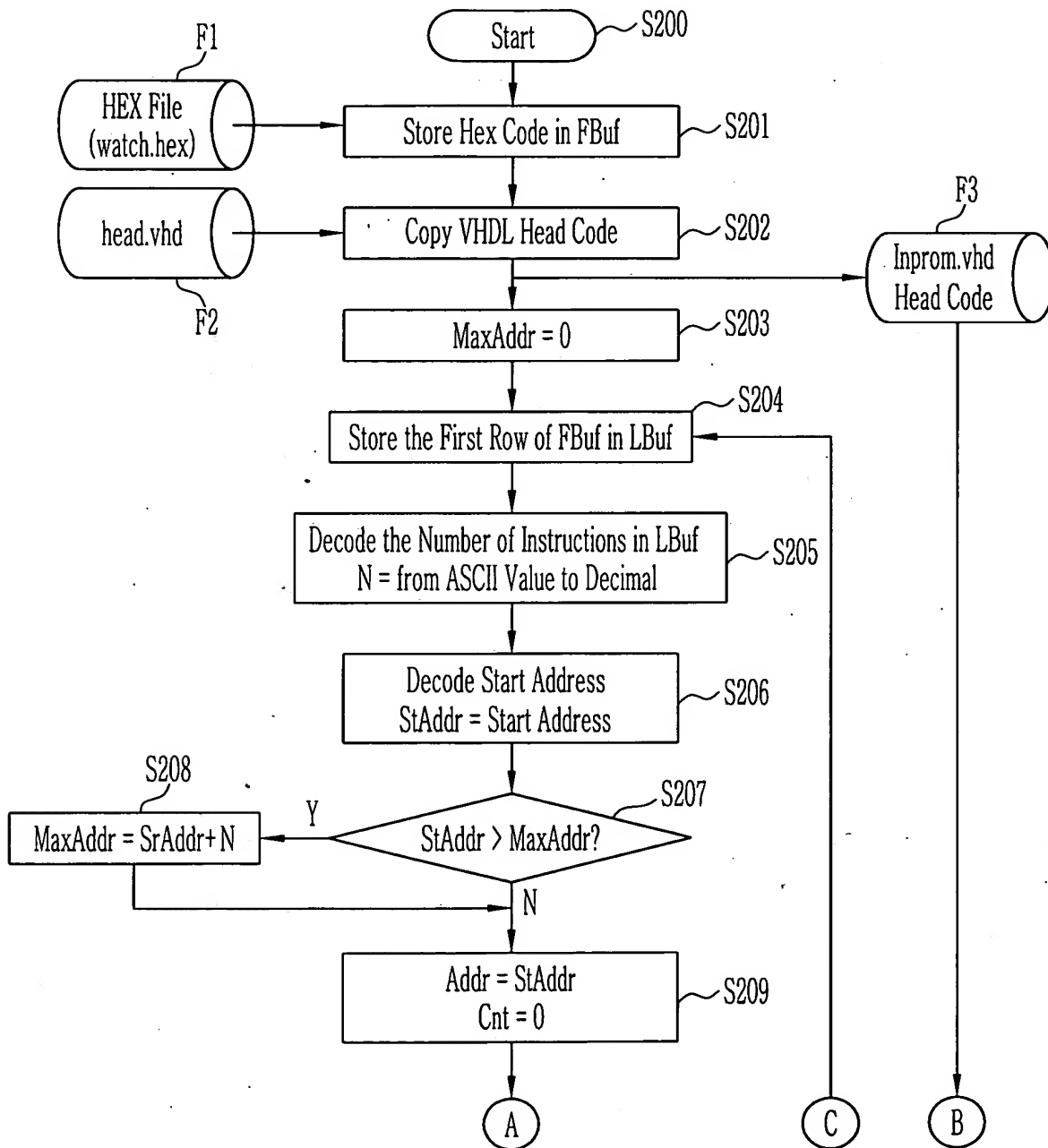


FIG. 6B

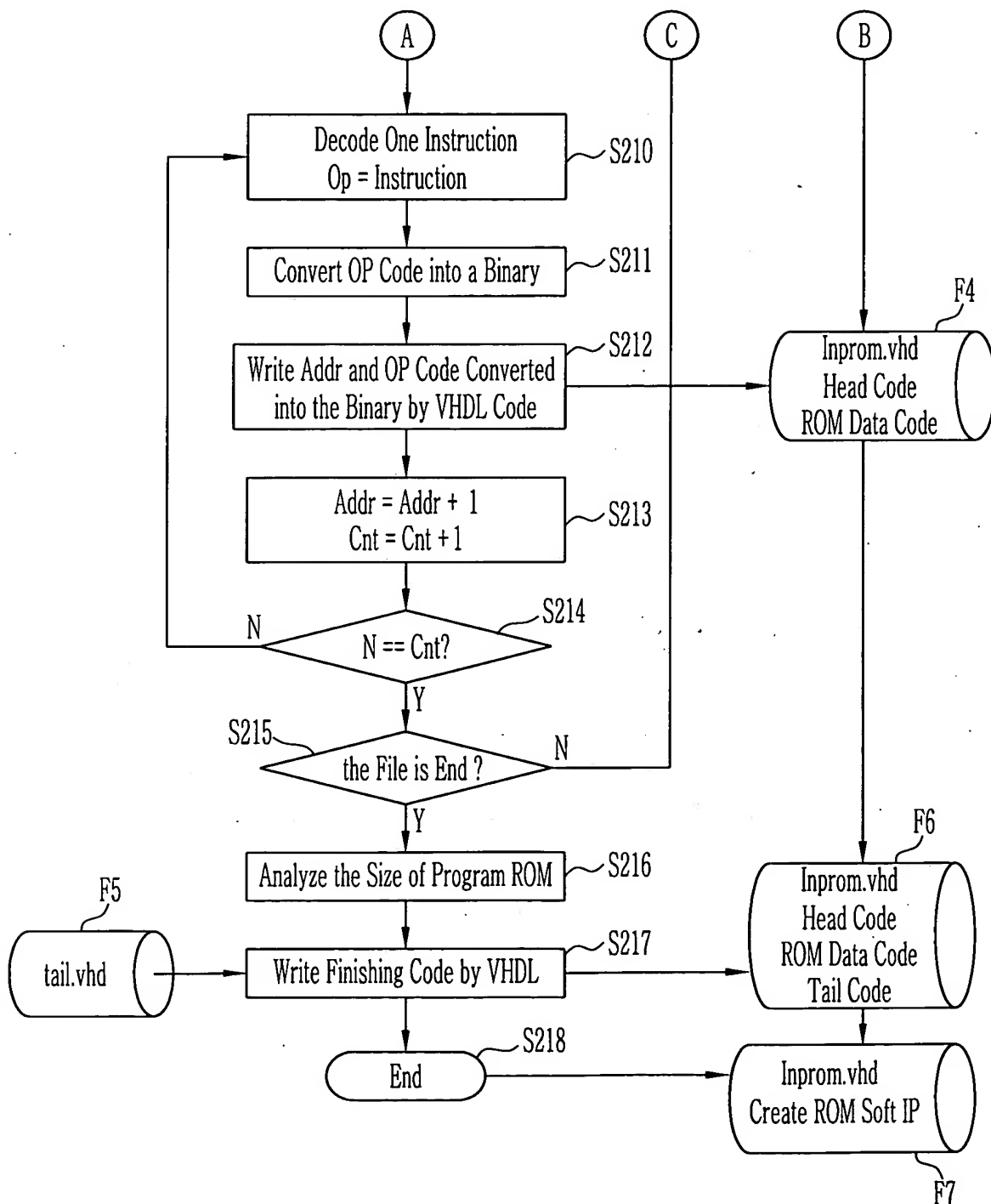


FIG. 7

```

LIBRARY ieee ;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
LIBRARY work ;
USE work.et8051_pkg.all;

ENTITY inprom IS
    PORT(
        addr : IN std_logic_vector (15 downto 0) ;
        dataout: OUT DATGBTYPE
    );
END inprom;

ARCHITECTURE behave OF inprom IS
    signal data : DATGBTYPE;
begin
    process (addr)
    begin
        case addr is
            when "0000000000000000" => data <= "00000010";
            when "0000000000000001" => data <= "00000000";
            when "0000000000000010" => data <= "00011110";
            when "0000000000001101" => data <= "00000010";
            when "0000000000011100" => data <= "00000000";
            when "0000000000011101" => data <= "01101101";
            when "0000000000011110" => data <= "01110101";
            when "0000000000011111" => data <= "00110000";
            when "0000000000100000" => data <= "00111111";
            when "0000000000100001" => data <= "01110101";
            when "0000000000100010" => data <= "00110001";
        end case;
    end process;
end behave;

```

Annotations in the image:

- Brackets A, B, and C group sections of the code.
- A large bracket on the right side of the code is labeled "Copied head code".
- A bracket on the right side of the case statement is labeled "Created ROM data: code(F4)".